IN THE SPECIFICATION

On page 1, after line 1 (Title of the Invention), please insert the following paragraph:

-- This Application is a Divisional Application of Serial No. 09/048,288 filed March 26, 1998.--

Please replace the second paragraph beginning on page 3, with the following rewritten paragraph:

-- In a MOS transistor prepared such that the stress of a channel layer is controlled by forming a multi-layered film based on the above property of the strain effect silicon layer, a high mutual conductance [gm (mobility)] can be obtained. Such a p-type MOS is disclosed in Appl. Phys. Letter (USA), 63 (1993) K. Ismail et al., p660 and IEEE Electronic Devices (USA), 43 (1996) L. H. Jiang and R. G. Elliman, p97. Further, an nMOS is disclosed in Appl. Phys. Letter (USA), 64 (1994) K. Ismail et al., p3124 and IEDM 94-37 (USA), (1994) J. Welser et al.--

Please replace the third paragraph beginning on page 5, with the following rewritten paragraph:

--In this field effect transistor, since the source/drain are formed only in the strain effect silicon layer, the junction of the source/drain is present in the strain effect silicon layer, to improve the mobility of the transistor, thereby improving the performance of the transistor.--

Please replace the third paragraph beginning on page 21, with the following rewritten paragraph:

--In the case of formation of the source/drain 14 and 15 having a LDD (Lightly Doped Drain) structure, after patterning of the gate, lightly doped diffusion layers for forming the LDD structure are formed in the strain effect silicon layer 24 are regions under side wall insulating films (formed later) by ion implantation. Then, side wall insulating films 17 and 18 are formed on side walls of the gate electrode 13, to form highly doped regions for the source/drain 14 and 15.--